CLAIMS

We claim:

1. A semiconductor structure comprising:

a substrate comprising a first relaxed semiconductor material with a first lattice constant;

a semiconductor device layer overlying the substrate, the semiconductor device layer comprising a second relaxed semiconductor material with a second lattice constant different from the first lattice constant; and

a dielectric layer interposed between the substrate and the semiconductor device layer, the dielectric layer having a programmed transition zone disposed within the dielectric layer for transitioning between the first lattice constant and the second lattice constant, the programmed transition zone comprising a plurality of layers, adjoining ones of the plurality of layers having different lattice constants with one of the adjoining ones having a first thickness exceeding a first critical thickness required to form defects and another of the adjoining ones having a second thickness not exceeding a second critical thickness, each adjoining layer of the plurality of layers forming an interface for promoting defects in the transition zone to migrate to an edge of the programmed transition zone.

2. The semiconductor structure of claim 1 wherein the programmed transition zone comprises a via having sidewalls that are substantially perpendicular to the substrate.

3. The semiconductor structure of claim 1 wherein the programmed transition zone comprises a via having sidewalls that are slanted and intersect with the substrate at an angle other than ninety degrees.

4. The semiconductor structure of claim 1 further comprising:

a strained material layer overlying the semiconductor device layer, the strained material layer having a thickness that is less than its critical thickness in order to minimize defects and maintain strain.

5. The semiconductor device of claim 4 further comprising:
a transistor control electrode overlying the strained material layer; and
transistor current electrodes positioned adjacent the strained material layer, the strained material layer functioning as a channel of the transistor.

6. The semiconductor device of claim 1 wherein a material composition of at least one of adjoining pairs of the plurality of layers differs from all other pairs of the plurality of layers.

7. The semiconductor device of claim 1 wherein the plurality of layers further comprise a plurality of pairs of transition layers, a first of each of the pairs of transition layers comprising a predetermined percentage of germanium wherein the predetermined percentage varies between at least two of the pairs of transition layers.

8. A semiconductor device structure comprising:
substrate means comprising a first relaxed material, the first relaxed material having a first lattice constant;
a dielectric layer means having an opening for defining a programmed transition zone to transition from the first relaxed material having the first lattice constant to a different lattice constant material, the programmed transition zone comprising a plurality of layers, each having a composition that is dissimilar from any adjoining layer of the plurality of layers to form an interface for promoting defects to migrate to an edge of the programmed transition zone, predetermined alternating layers of the plurality of layers having a thickness that exceeds a critical thickness for its material composition to form defects to relieve strain, and intervening layers of the plurality of layers having a thickness that does not exceed a critical thickness for its material composition to be strained, wherein an upper layer of the plurality of layers is substantially defect free; and
a semiconductor device layer means overlying at least the programmed transition zone, the semiconductor device layer means comprising a second relaxed material having a second lattice constant that is the different lattice constant material.

9. The semiconductor device structure of claim 8 further comprising:

a strained material layer means overlying the semiconductor layer means, the strained material layer means functioning as a material having increased charge carrier mobility for an element of the semiconductor device structure.

10. The semiconductor device structure of claim 9 wherein the strained material layer means further comprise strained silicon.

11. The semiconductor device structure of claim 9 further comprising:

transistor control electrode means overlying the strained material layer means; and

current electrode means formed within the semiconductor device layer means and adjoining the transistor control electrode means to form a transistor wherein the strained material layer means functions as a channel of the transistor.

12. The semiconductor device structure of claim 8 wherein the programmed transition zone further comprises:

a first of the plurality of layers overlying the substrate means and comprising one of silicon germanium, gallium arsenide and aluminum arsenide;

a second of the plurality of layers overlying the first of the plurality of layers, the second of the plurality of layers comprising one of silicon germanium carbon, silicon carbon, silicon, silicon germanium, gallium arsenide and aluminum arsenide;

a third of the plurality of layers overlying the second of the plurality of layers, the third of the plurality of layers comprising one of silicon germanium carbon, silicon carbon, silicon, silicon germanium, gallium arsenide and aluminum arsenide;

a fourth of the plurality of layers overlying the third of the plurality of layers, the fourth of the plurality of layers comprising one of silicon germanium, gallium arsenide and aluminum arsenide; and

one or more additional layers of the plurality of layers overlying the fourth of the plurality of layers, a final of the one or more additional layers being a substantially defect free material.

13. The semiconductor device structure of claim 8 wherein the programmed transition zone further comprises:

a via formed in the dielectric layer means, the via having sidewalls that are non-orthogonal to the substrate means.

14. The semiconductor device structure of claim 8 wherein the substrate means further comprise a material composed of one of silicon, gallium arsenide, aluminum arsenide, gallium phosphorous and indium phosphorous.

15. A method of forming a semiconductor device structure comprising:

forming a substrate means comprising a first relaxed material, the first relaxed material having a first lattice constant;

forming a dielectric layer means overlying the substrate means, the dielectric layer means having an opening for defining a programmed transition zone to transition from the first relaxed material having the first lattice constant to a different lattice constant material;

forming the programmed transition zone with a plurality of layers, each of the plurality of layers comprising a composition that is dissimilar from any adjoining layer of the plurality of layers to form an interface for promoting defects to migrate to an edge of the programmed transition zone;

forming predetermined alternating layers of the plurality of layers with a thickness that exceeds a critical thickness for its material composition to form defects to relieve strain;

forming intervening layers of the plurality of layers that intervene the predetermined alternating layers with a thickness that does not exceed a critical thickness for its material composition to be strained, wherein an upper layer of the plurality of layers is substantially defect free; and

forming a semiconductor device layer means overlying at least the programmed transition zone, the semiconductor device layer means comprising a second relaxed material having a second lattice constant that is the different lattice constant.

16. The method of claim 15 further comprising:
forming a strained material layer overlying the semiconductor device layer means, the strained material layer formed with a thickness that is less than its critical thickness in order to minimize defects and maintain strain.

17. The method of claim 15 further comprising:
forming a transistor by forming current electrode diffusions within the semiconductor device layer means and forming a gate electrode overlying and separated from the strained material layer by a dielectric layer means, the strained material layer functioning as a channel of the transistor.

18. The method of claim 15 further comprising:
epitaxially growing each of the plurality of layers.

19. A method of forming a semiconductor device comprising:
providing a substrate comprising a first relaxed semiconductor material with a first lattice constant;
providing a semiconductor device layer overlying the substrate, the semiconductor device layer comprising a second relaxed semiconductor material with a second lattice constant different from the first lattice constant; and
interposing a dielectric layer between the substrate and the semiconductor device layer, the dielectric layer having a programmed transition zone disposed within the dielectric layer for transitioning between the first lattice constant and the second lattice constant; and
forming the programmed transition zone with a plurality of layers, adjoining layers of the plurality of layers having different lattice constants with one of each of the adjoining layers having a first thickness exceeding a first critical thickness required to form defects and another of each of the adjoining layers having a second thickness not exceeding a second critical thickness, each adjoining layer of the plurality of layers forming an interface for promoting defects in the transition zone to migrate to an edge of the programmed transition zone, an upper surface of the programmed transition zone being substantially free of defects.

20. The method of claim 19 further comprising:
forming a strained material layer overlying the semiconductor device layer, the strained material layer having a thickness that is less than its critical thickness in order to minimize defects and maintain strain.

21. The method of claim 19 further comprising:
forming a transistor within the semiconductor device layer and overlying the strained material layer, the transistor comprising a source and a drain implanted within the semiconductor device layer and comprising a gate overlying the strained material layer, the strained material layer functioning as a channel of the transistor.